IN THE CLAIMS:

The claims are amended as follows:

1. (Currently Amended) A method for refreshing a dynamic memory cell in a memory circuit, the memory cell being arranged at a word line and a bit line of a bit line pair, comprising:

during read-out of the memory cell, activating the word line and ~~separating~~ amplifying, with a sense amplifier, a charge difference brought about thereby on the bit lines ~~into~~ to generate a high charge potential and a low charge potential;

after the read-out, charging the potentials of the bit lines to a first center potential;

during refresh of the memory cell, activating the word line and ~~separating~~ amplifying, with the sense amplifier, the charge potentials of the bit lines, depending on [[the]] charge information of the memory cell, ~~in the direction of~~ to generate a high refresh potential and a low refresh potential; and

after the refresh, charging the potentials of the bit lines to a second center potential, wherein the potential difference between the high refresh potential to which the sense amplifier drives the bit lines during refresh and the second center potential is greater than the potential difference between the high charge potential to which the sense amplifier drives the bit lines during readout and the first center potential.

2. (Original) The method of claim 1, wherein the high refresh potential is greater than the high charge potential.

3. (Original) The method of claim 2, wherein the first center potential lies between the low and the high refresh potentials.

4. (Original) The method of claim 1, wherein the first and second center potentials are substantially equal.

5. (Original) The method of claim 1, wherein the first center potential is greater than the second center potential.

6. (Original) The method of claim 1, wherein the word line remains activated for a shorter time duration during the refresh than during the read-out.

7. (Original) The method of claim 1, wherein the refresh of the memory cell is carried out in a self-refresh operation.

8. (Original) The method of claim 1, wherein a time duration of the refresh period after which the memory cell is periodically refreshed is increased after a first refresh following a write or read access to the memory cell.

9. (Original) The method of claim 8, wherein, during the refresh, the word line is activated only until that bit line which has the higher potential has a charge potential which is higher, by a defined potential magnitude, than the charge potential the bit line has after a write or read access.

10. (Original) A memory circuit, comprising:

a memory cell array with a memory cell arranged at a word line and a bit line pair;

a refresh circuit for generating signals to refresh the memory cell;

a charge equalization circuit to charge the bit lines to a common center potential after a read-out or refresh of the memory cell;

a sense amplifier in order to separate a charge difference between the bit lines into a high charge potential and a low charge potential when the wordline is activated during a read-out or refresh of the memory; and

voltage control means for varying the potential difference between the high charge potential and the common center potential, wherein the potential difference between the high charge potential and the common center potential during a refresh of

the memory cell is greater than the potential difference between the high charge potential and the common center potential during a read-out of the memory cell.

11. (Original) The memory circuit of claim 10, wherein the voltage control means provides the sense amplifier with the high charge potential from a first high potential source during refresh of the memory cell and from a second high potential source during read-out of the memory cell.

12. (Original) The memory circuit of claim 11, wherein the voltage control means comprises a switch connectable to the first high potential source in response to a signal provided by the refresh circuit.

13. (Original) The memory circuit of claim 10, wherein the voltage control means provides the charge equalization circuit with the common center potential from a first center potential source during refresh of the memory cell and from a second center potential source during read-out of the memory cell, wherein the first center potential is less than the second center potential.

14. (Original) The memory circuit of claim 10, wherein the word line remains activated for a shorter time duration during the refresh than during the read-out.

15. (Original) The memory circuit of claim 14, wherein a time duration of the refresh period after which the memory cell is periodically refreshed is increased after a first refresh following a write or read access to the memory cell.

16. (Original) The memory circuit of claim 14, wherein, during the refresh, the word line is activated only until that bit line which has the higher potential has a charge potential which is higher, by a defined potential magnitude, than the charge potential the bit line has after a read-out

17. (Currently Amended) A memory circuit, comprising:

a memory cell array with a memory cell arranged at a word line and a bit line pair;

a refresh circuit for generating signals to refresh the memory cell;

a charge equalization circuit to charge the bit lines to a common center potential after a read-out or refresh of the memory cell;

a sense amplifier in order to separate a charge difference between the bit lines into a high charge potential and a low charge potential when the wordline is activated during a read-out or refresh of the memory;

first and second potential sources, wherein the first potential source is greater than the second potential source; and

a voltage control circuit configured to provide[[s]] the sense amplifier with the high charge potential from the first potential source during refresh of the memory cell and from a second high potential source during read-out of the memory cell.

18. (Original) The memory circuit of claim 17, wherein the voltage control circuit comprises a switch connectable to the first potential source in response to a signal provided by the refresh circuit.

19. (Original) The memory circuit of claim 17, further comprising:

third and fourth potential sources, wherein the third potential source is lower than the fourth potential source; and

wherein the voltage control circuit is configured to provide the charge equalization circuit with the common center potential from the third potential source during refresh of the memory cell and from the fourth potential source during read-out of the memory cell.